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SIMULATION AND DESIGN OF HETEROGENEOUS FIR DIGITAL FILTER FOR DSP APPLICATION USING VHDL

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ABSTRACT

An adder is the fundamental building block of the digital circuits such as ALU, microprocessors and microcontrollers, DSP processors and several arithmetic operations. Full adder is the main part of the arithmetic circuits. Full adder circuit is the basic cell of arithmetic circuits. Many applications need logic circuits of small chip area, high throughput, and low power utilization. The paper is focused on the design of 16-bit ripple carry adder based on homogeneous adder-based concept. The chip design is done in Xilinx ISE 14.2 using VHDL and simulated in Modelsim 10.1 software. The design is synthesized on SPARTAN - 3E FPGA to verify the results.

KEYWORDS: Ripple Carry Adder, Digital Signal Processing, FPGA, VHDL programming

1. INTRODUCTION

Adders are the basic building blocks of the digital applications and computing of microprocessors. The adders used for these systems are half adder and full adder. Half adder and full adder [1, 2] are the combinational circuit that provides the sum of two bit binary and three bits binary respectively and provides the sum and carry. The larger bit data is added by parallel adder or the ripple carries adder. The adder is used for different DSP applications such as filter design [3]. The full adder is the basic component of the ripple carry adder. Full adder [4, 5] is combinational logic which is accepting 3 binary bits to provide sum and carry as the output. The logic diagram is shown in fig 1 and behaviour of full adder is shown in table 1. The logical expressions are presented with the help of equ.(1) and equ.(2).

Table 1 Truth table of full adder

Input			**Output**	
a	**B**	**C**	**sum**	**carry**
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

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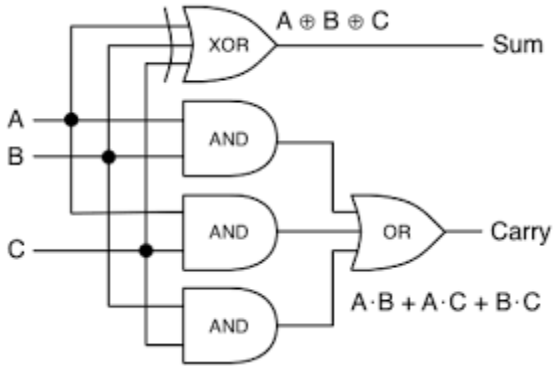

Fig. 1 Logic diagram of full adder

$$sum = \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} + abc = a \oplus b \oplus c \quad (1)$$

$$carry = \bar{a}bc + a\bar{b}c + ab\bar{c} + abc = ab + bc + ca \quad (2)$$

2. RIPPLE CARRY ADDER (RCA)

The design of the FIR filter [8, 10] is carried out using Ripple Carry Adder (RCA) instead of the decimal adder. The RCA will accept the 4-bit data as shown in Fig. 3 The 4-bit adder using full adder circuits can add two 4-bit numbers resulting in a 4-bit sum and a carry. Hence the sum by each full adder is performed simultaneously. This circuit is called the parallel adder or ripple carry adder. In a 4-bit parallel binary adder circuit, the input of each full adder will be A_i, B_i, and C_i, and the outputs will be S_i and C_{i+1}, where i vary from 0 to 3. The carry of the previous stage is associated with a carry input of the succeeding stage. In the first stage A_0, B_0 and C_0 (or $C_0 = C_{in}$, which is 0) are added resulting sum S_0 and carry C_1. This carry C_1 becomes the carry input to the second stage.

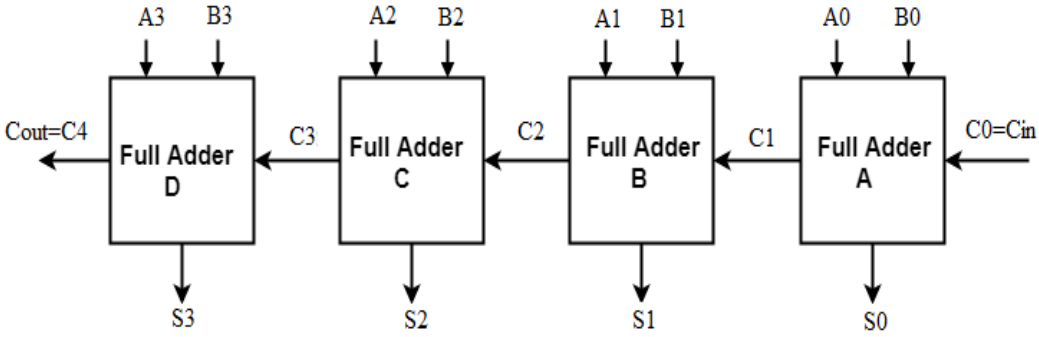

Fig. 2 Four-bit binary adder or Parallel binary adder

In the same way, the second stage A_1, B_1 and C_1 are added resulting S_1 and C_2. Carry C_2 is the input for the third stage. A_2, B_2, and C_2 are added resulting S_2 and C_3. Carry C_3 is carried in the fourth stage. A_3, B_3, and C_3 are added and resulting in S_3 and C_4. Here, C_4 acts as a carry-out or C_{out}. Thus, this circuit results in a sum ($S_3S_2S_1S_0$) and a carry C_{out}.

3. REALIZATION OF 16-BIT HOMOGENOUS ADDER

In the same way, 16-bit ripple adder can be designed using either direct 16 number of full adders based on the concept of 4-bit RCA or it is also possible to use the cascade structure shown in the Fig. 4. In which 4 RCA are used in which RCA1 performs the addition of x(3:0) and y(3:0), RCA2 adds x(7:4) and y(7:4), RCA3 adds x(11:8) and y(11:8) and RCA4 performs x(15:12) and y(15:12). The output of the RCA1, RCA2, RCA3 and RCA4 give the out of sum Sout (3:0), Sout (7:4), Sout (11:8), and Sout (15:12). The output carry of one RCA is given as the input to the next RCA. In the RCA as the length

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increases, there are the chances that the delay will increase. The delay calculation for the 'N' bit RCA is given by the Eq. (3)

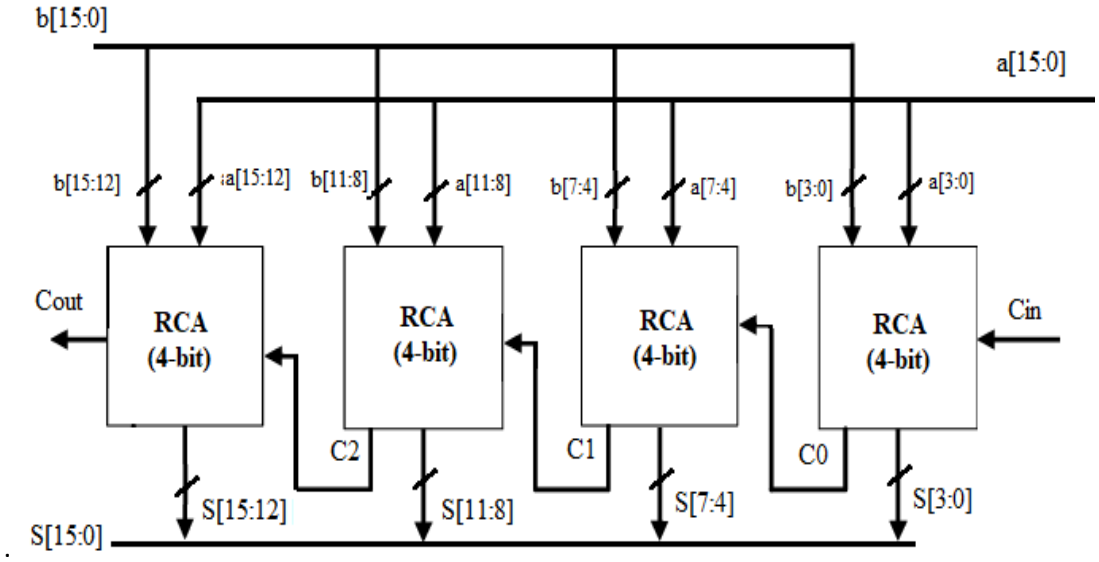

Fig. 3 Homogenous adder-based structure (16 bit)

$$T_{logic} = T_{Fulladder}\left((x_{0,}\, y_0)\ to\ c_0\right) + (n-2) \times T_{Fulladder}(C_{in}\ to\ C_{out}) + T_{Fulladder}(C_{in}\ to\ S_{out}(n-1)) \quad (4.3)$$

In this equation, $T_{FullAdder}$ presents the delay of the full adder for the specified input and output with respect to the path of I/O.

4. RESULTS & DISCUSSIONS

The Xilinx software provides the RTL of the developed chip of adder which is depicted in the fig. 4 and internals schematic is also presented in the fig.5. The RTL provides the complete information of the input and output pins used in the design. The description of all the pins is given in table 2. The waveform simulation of the same is given in fig.6

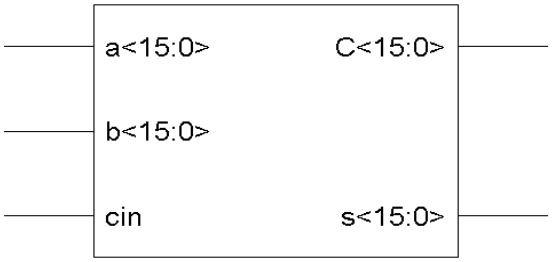

Fig.4 RTL view of adder

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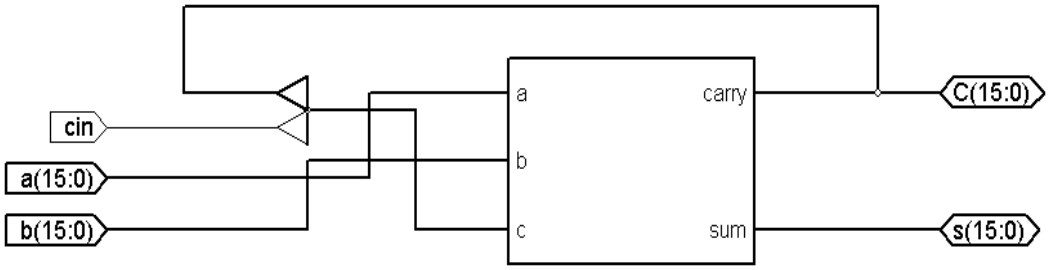

Fig.5 Internal schematic of 16-bit adder

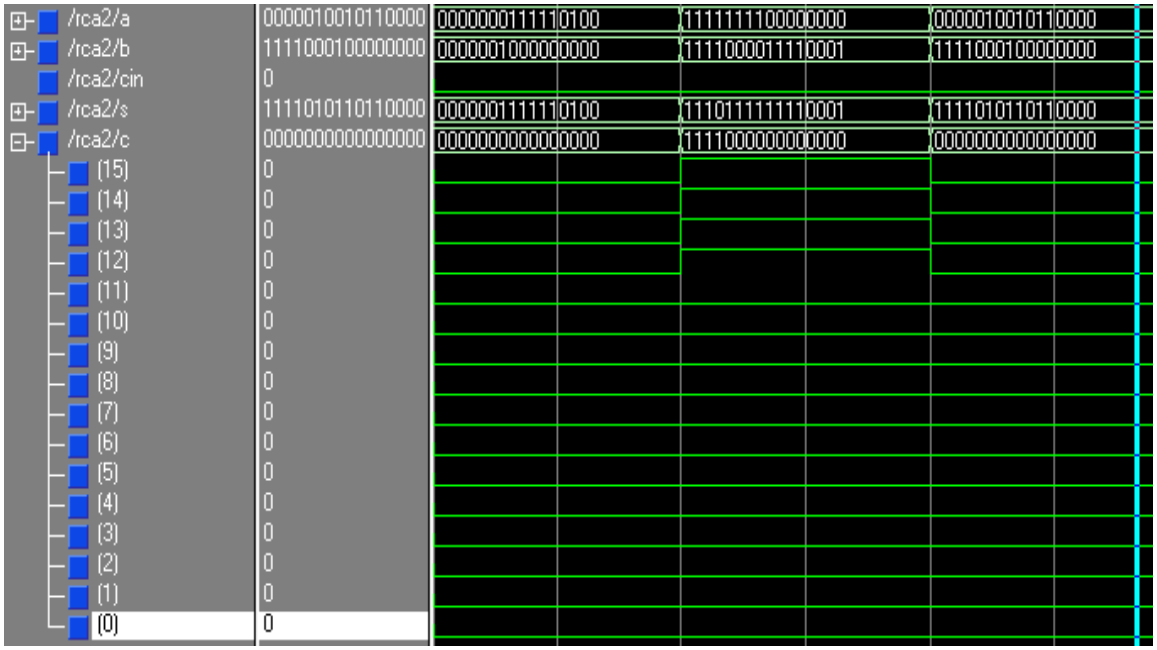

Fig.6 Modelsim waveform simulation of 16-bit adder

Test input-1: a = 0000000111110100 and b = 0000001000000000 then output s = 0000001111110100
Test input-2: a = 1111111100000000 and b = 1111000011110001 then output s = 1111000000000000
Test input-3: a = 0000010010110000 and b = 1111000100000000 then output s = 1111010110110000

Table 2 Pin details of the chip

Pin	Description
A[15:0]	It is the first 16-bit input of the adder. It is of the std_logic_vector data type.
B[15:0]	It is the second 16-bit input of the adder. It is of the std_logic_vector data type.
Cin	It is the input carry, considered as Cin = 0. It is of std_logic.
S[15:0]	It is the adder output of 16-bit. It is of the std_logic_vector data type.
C[15:0]	It is 16-bit outputs considered as an intermediate carry of the adder including output carry as C[15]. It is of the std_logic_vector data type.

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The Xilinx software gives the details of the hardware utilization for the homogenous adder based 16-bit ripple carry adder. The table 3 provides the details of hardware summary and timing values. The hardware parameter slices, LUTs, memory and bounded input/output (IoBs), and 1-bit XOR2. Fig.7 presents the graph for the hardware resources. The combinational time presents the logic delay and routing delay from input to output. The information is directly extracted from the software with the target device on SPARTAN 3E FPGA.

Table 3 Xilinx software parameters for 16- bit adder

Parameter	16-bit Homogenous Adder
Slices Usage	23
LUTs Usage	40
IoBs	65
1 bit XOR2	16
Memory Usage	111572 kB
Combinational time	36.323 ns

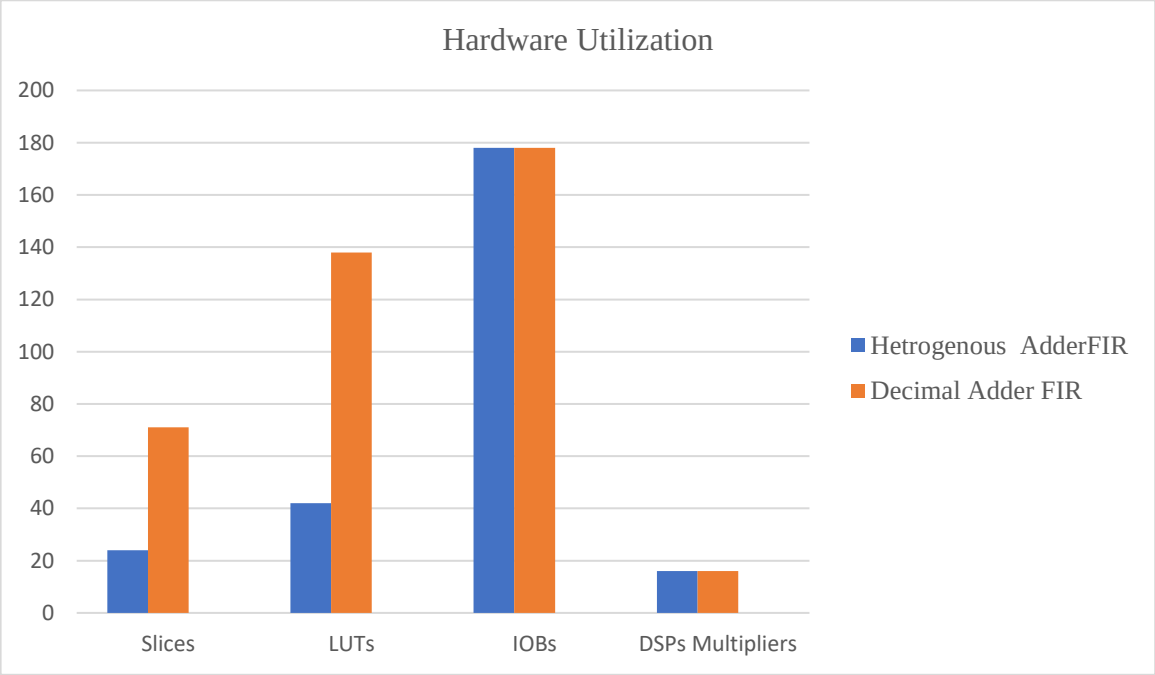

Fig.7 Hardware usage curve with different parameters

5. CONCLUSIONS

The design of 16-bit homogenous ripple carry adder is done in Xilinx ISE 14.2 successfully. The output of the adder is simulated for many cases in modelsim10.1 software. The design is based on cascading approach of same type of full adders circuits to form the 4 bit ripple carry adder and further use to implement the 16 bit adder. The such design is applicable in several digital circuit and DSP based communication system. The designed chip is synthesized successfully on SPARTAN-3E FPGA and device parameters such slices, device LUT, IoBs, XOR gate are 23, 40, 65 and 16 respectively. The design is using the memory 111572 kB and combinational path time is 36.323 ns. The developed chip will be beneficial for the signal processing applications in which addition is the building blocks and computations are needed such as FIR filter design, DFT algorithm, FFT computations in which large scale adders are multipliers are used.

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REFERENCES

[1] Krishna, O. V., 2018. Design and Implementation of FIR Filter using Low Power and High-Speed Multiplier and Adders. CVR Journal of Science and Technology, 15, 80-84.
[2] Dinis, D. C., Cordeiro, R. F., Oliveira, A. S., Vieira, J., & Silva, T. O., "A fully parallel architecture for designing frequency-agile and real-time reconfigurable FPGA-based RF digital transmitter", IEEE Transactions on Microwave Theory and Techniques, 66(3), 1489-1499,2018.
[3] Ambede, A., Shreejith, S., Vinod, A. P., & Fahmy, S. A. "Design and realization of variable digital filters for software-defined radio channelizers using an improved coefficient decimation method". IEEE transactions on circuits and systems ii: EXPRESS BRIEFS 63, no. 1 (2016): 59-63.
[4] Mahendran, N., & Vishwaja, S., "Performance Analysis of High-Speed Adder for DSP Applications", World Academy of Science, Engineering and Technology, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, 10(3), 464-469, 2016.
[5] Sharma, P., Gupta M., "Area-Efficient Implementation of Heterogeneous Adder and its Application in FIR Filter", International Journal of Research in Electronics and Computer Engineering, Vol.3, 2015, pp (1-5).
[6] S. Asad Alam and O. Gustafsson "Design of Finite Word Length Linear-Phase FIR Filters in the Logarithmic Number System Domain" Hindawi Publishing Corporation VLSI Design Volume 2014, Article ID 217495, pp(1-14).
[7] Park, S. Y., & Meher, P. K., "Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter", IEEE Transactions on Circuits and Systems II: Express Briefs, 61(7), 511-515, 2014.
[8] Singh, R. P. P., Chaturvedi, A., & Singh, O., 2012. Trade-offs in Designing High-Performance Digital Adder based on Heterogeneous Architecture. International Journal of Computer Applications, 56(13).
[9] Qasim, S. M., BenSaleh, M. S., Bahaidarah, M., AlObaisi, H., AlSharif, T., AlZahrani, M., & AlOnazi, H., 2012. Design and FPGA implementation of sequential digital FIR filter using microprogrammed controller. In 2012 IV International Congress on Ultra-Modern Telecommunications and Control Systems, pp. 1002-1005, IEEE.
[10] Mahesh, R., & Vinod, A. P., "New reconfigurable architectures for implementing FIR filters with low complexity", IEEE transactions on computer-aided design of integrated circuits and systems, 29(2), 275-288, 2010.
[11] Devi, P., Girdher, A., & Singh, B., "Improved carry select adder with reduced area and low power consumption", International journal of computer applications, 3(4), 14-18, 2010.
[12] Lin, M. C., Chen, H. Y., & Jou, S. J. Design techniques for high-speed multirate multistage FIR digital filters. International journal of electronics, 93(10), 699-721, 2006.